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VEDDER PRICE KAUFMAN & KAMMHOLZ
222 N. LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	
ART UNIT	**PAPER NUMBER**
2671	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,484	CALLWAY, EDWARD G.	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-39 is/are pending in the application.

4a) Of the above claim(s) 2-17 and 23-28 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,18,19,21,22 and 29-39 is/are rejected.

7)☒ Claim(s) 20 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/19/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on November 16, 2004 was filed after the mailing date of the application on October 17, 2001. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

2. In light of Applicant's amendment to the abstract, the objection to the abstract has been withdrawn.

3. In light of Applicant's amendment to Claim 30, the objection to the claim has been withdrawn.

4. In light of Applicant's amendment to Claim 22, the rejection under 35 U.S.C. 112, second paragraph, of the claim has been withdrawn.

5. Applicant's arguments with respect to claims 1, 18-22, 29-39 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's arguments, see pages 7-12, filed February 28, 2005, with respect to the rejection of claims 1 and 19 under 35 U.S.C. 102(b) and the rejections of claims 18, 20-22, and 29-39 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Normile (US005461679A), Jordan (US006028643A), Gonsalves (US006847373B1), and Taylor (US006118461A).

7. With regard to Claim 1, Applicant argues that memory 101 of the Grigor reference is not a "video output port" (page 7, lines 22-24).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Normile. Normile describes a video driver system comprising a first graphics device (401, Figure 4, *video processing module*, Col. 9, lines 11-15) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (412) to provide a first video output component signal (*modules 401-404 are coupled to a computer system bus 425 via control bus 412...coupled to system bus 425 is display controller 426...information is placed onto bus 425 by modules 401-404 and read in by display controller 426*, Col. 9, lines 15-24); a second graphics device (402, *video processing module*, Col. 9, lines 11-15) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (412) to provide a first video output component signal; a first video output port (425) coupled to the first video component output of the first graphics device and the first video component output of the second graphics device (*modules 401-404 are coupled to a computer system bus 425 via control bus*

412...coupled to system bus 425 is display controller 426...information is placed onto bus 425 by modules 401-404 and read in by display controller 426, Col. 9, lines 15-24); and a second video output port (440) coupled to the first video component output of the second graphics device (Col. 10, lines 7-19).

8. With regard to Claim 18, Applicant argues that this claim is allowable for the same reasons given with respect to Claim 1 (page 8, line 24-page 9, line 3).

In reply, the Examiner disagrees that Claim 18 is allowable for the same reasons given with respect to Claim 1.

9. With regard to Claim 19, Applicant argues that that the Z value of Hung is not a video output component as known in the art (page 8, lines 15-21).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Jordan and Gonsalves. Jordan describes a method of providing a video signal (*displaying video information*, Col. 2, lines 35-37), the method comprising generating a first signal at a first device (210, Figure 2), wherein the first signal is representative of a first video output component (*resultant data from the accelerators 210, 235 is output*, Col. 6, lines 45-47); providing the first signal to a first node; determining a value of the first signal at a first output node (247, Figure 2A; *resultant data from the accelerators 210, 235 is output to the computer monitors 130, 140 via video monitor interface components 245, 255*, Col. 6, lines 45-47, Col. 5, lines 62-64); generating a second signal at a second device (235, Figure 2), wherein the second signal is representative of a first video output component (*resultant data from the accelerators 210, 235 is*

output, Col. 6, lines 45-47); providing the second signal of the second device to the first output node (*resultant data from the accelerators 210, 235 is output to the computer monitors 130, 140 via video monitor interface components 245, 255*, Col. 6, lines 45-47, Col. 5, lines 62-64), as can be seen in Figure 2A.

Gonsalves describes making color modifications to correct color errors due to process errors (Col. 1, lines 26-29). Such corrections include matching colors and tones from shot to shot (Col. 1, lines 34-38). Gonsalves describes adjusting the values of the selected destination color component for color matching (Col. 3, lines 42-50; Col. 24, lines 16-19).

10. With regard to Claims 21 and 22, Applicant argues that these claims are allowable for the same reasons given with respect to Claim 19 (page 9, lines 4-10).

In reply, the Examiner disagrees that Claims 21 and 22 are allowable for the same reasons given with respect to Claim 19.

11. With regard to Claim 29, Applicant argues that in Kehlet, none of the devices outputs the same video and none of the graphics accelerators output video to a common port as none of the accelerators are used to couple to the same display device (page 10, lines 1-3). In Emery, the CPUs output portions of the same frame to a single output port (page 10, lines 12-13). Therefore, the combination of Kehlet and Emery fail to disclose two different graphics devices that each render a different frame of video where one renders one frame and the other renders an adjacent frame (page 10, lines 16-18).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Normile and Taylor. Normile was discussed above with regard to Claim 1. Taylor describes two display control units (103, Figure 1, Col. 4, lines 14-18), and each display control unit includes a display controller (104) and a frame buffer (105) (Col. 4, lines 19-21). A display controller is a VGA controller (Col. 4, line 49) and executes a limited number of graphics functions such as line draws, polygon fills, color space conversion, display data interpolation and zooming (Col. 4, lines 52-57). Taylor describes that the frame from the frame buffer of display control unit 103a (Col. 5, line 65-Col. 6, line 1) is output first to the display (110) (Col. 6, lines 50-61), then the frame from the frame buffer of display control unit 103b (Col. 5, line 65-Col. 6, line 1) is output next to the display (Col. 7, lines 11-30). Therefore, Taylor describes that the first graphics device renders a frame of video and provides the rendered frame to the first video output port, and that the second graphics device renders an adjacent frame of video and provides the adjacent frame to the first video output port.

12. With regard to Claims 30-39, Applicant argues that these claims are allowable for the same reasons given with respect to Claim 29 (pages 11-12).

In reply, the Examiner disagrees that Claims 30-39 are allowable for the same reasons given with respect to Claim 29.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Normile (US005461679A).

15. With regard to Claim 1, Normile describes a video driver system comprising a first graphics device (401, Figure 4, *video processing module*, Col. 9, lines 11-15) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (412) to provide a first video output component signal (*modules 401-404 are coupled to a computer system bus 425 via control bus 412...coupled to system bus 425 is display controller 426...information is placed onto bus 425 by modules 401-404 and read in by display controller 426*, Col. 9, lines 15-24); a second graphics device (402, *video processing module*, Col. 9, lines 11-15) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (412) to provide a first video output component signal; a first video output port (425) coupled to the first video component output of the first graphics device and the first video component output of the second graphics device (*modules 401-404 are coupled to a computer system bus 425 via control bus 412...coupled to system bus 425 is display controller 426...information is placed onto bus 425 by modules 401-404 and read in by display controller 426*, Col. 9, lines 15-24); and a second video output port (440) coupled to the first video component output of the second graphics device (Col. 10, lines 7-19).

16. With regard to Claim 18, Normile describes a monitor (428, Figure 4) coupled to the first video output port (426, *read in by display controller 426 for placing into frame buffer 427 and display on 428*, Col. 9, lines 19-24).

17. Thus, it reasonably appears that Normile describes or discloses every element of Claims 1 and 18 and therefore anticipates the claims subject.

18. Claims 30, 31, 38, and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Taylor (US006118461A).

19. With regard to Claim 30, Taylor describes that the frame from the frame buffer of display control unit 103a (Col. 5, line 65-Col. 6, line 1) is output first to the display (110) (Col. 6, lines 50-61), then the frame from the frame buffer of display control unit 103b (Col. 5, line 65-Col. 6, line 1) is output next to the display (Col. 7, lines 11-30). Therefore, Taylor describes an apparatus for providing video signals comprising a first graphics device operative to render a first frame of video and a second graphics device operative to render a second frame of video. Taylor describes a common port (109), operatively coupled to receive the first and second frames of rendered video from either of the first and second graphics devices (*display driver 109 receives digital data from controller 104*, Col. 5, lines 1-3), as can be seen in Figure 1.

20. With regard to Claim 31, Taylor describes a first frame buffer operatively coupled to the first graphics device and a second frame buffer operatively coupled to the second graphics device (*two display control units 103, Col. 4, lines 14-18, each display control unit 103 includes a frame buffer 105*, Col. 4, lines 19-21).

21. With regard to Claim 38, Taylor describes that the first graphics device and second graphics devices (*two display control units 103*, Col. 4, lines 14-18) are video graphics adapters (*each display control unit 103 includes a display controller 104, Col. 4, lines 19-20, display controller 104 may be VGA controller*, Col. 4, line 49).

22. With regard to Claim 39, Taylor describes that the frame from the frame buffer of display control unit 103a (Col. 5, line 65-Col. 6, line 1) is output first to the display (110) (Col. 6, lines 50-61), then the frame from the frame buffer of display control unit 103b (Col. 5, line 65-Col. 6, line 1) is output next to the display (Col. 7, lines 11-30). Therefore, Taylor describes that the first and second rendered frames are adjacent frames of video.

23. Thus, it reasonably appears that Taylor describes or discloses every element of Claims 30, 31, 38, and 39 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

26. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jordan (US006028643A) in view of Gonsalves (US006847373B1).

Jordan describes a method of providing a video signal (*displaying video information*, Col. 2, lines 35-37), the method comprising generating a first signal at a first device (210, Figure 2), wherein the first signal is representative of a first video output component (*resultant data from the accelerators 210, 235 is output*, Col. 6, lines 45-47); providing the first signal to a first node; determining a value of the first signal at a first output node (247, Figure 2A; *resultant data from the accelerators 210, 235 is output to the computer monitors 130, 140 via video monitor interface components 245, 255*, Col. 6, lines 45-47, Col. 5, lines 62-64); generating a second signal at a second device (235, Figure 2), wherein the second signal is representative of a first video output component (*resultant data from the accelerators 210, 235 is output*, Col. 6, lines 45-47); providing the second signal of the second device to the first output node (*resultant data*

from the accelerators 210, 235 is output to the computer monitors 130, 140 via video monitor interface components 245, 255, Col. 6, lines 45-47, Col. 5, lines 62-64), as can be seen in Figure 2A.

However, Jordan does not teach adjusting the second device until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node. However, Gonsalves describes making color modifications to correct color errors due to process errors (Col. 1, lines 26-29). Such corrections include matching colors and tones from shot to shot (Col. 1, lines 34-38). Gonsalves describes adjusting the values of the selected destination color component for color matching (Col. 3, lines 42-50; Col. 24, lines 16-19). Therefore, combining Jordan and Gonsalves, it would be obvious to adjust the second device until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Jordan to include adjusting the second device until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node as suggested by Gonsalves because Gonsalves suggests the advantage of correcting color errors due to process errors (Col. 1, lines 26-29).

27. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jordan (US006028643A) in view of Gonsalves (US006847373B1), further in view of Krenik (US005596583A).

Jordan and Gonsalves are relied upon for the teachings as discussed above relative to Claim 19.

However, Jordan and Gonsalves do not specifically teach that the value of the first and second signals is a voltage value. However, Krenik describes test circuitry for graphics processors that has a comparator circuit (141, Figure 6d) that makes voltage comparisons (Col. 9, lines 33-46).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Jordan and Gonsalves so that the value of the first and second signals is a voltage value as suggested by Krenik because the comparator inherently can only read voltage values. Using a comparator to make voltage comparisons is well-known in the art and can be found in many publications.

28. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jordan (US006028643A) in view of Gonsalves (US006847373B1), further in view of Davis (US006009487A).

Jordan and Gonsalves are relied upon for the teachings as discussed above relative to Claim 19.

However, Jordan and Gonsalves do not teach that the step of determining includes the substep of modifying and comparing the value of the first device until the value of the first signal substantially matches a predetermined value. However, Davis describes a video driver system comprising a master graphics controller (11, Figure 1) and slaves (12; Col. 4, lines 51-59). Davis

describes modifying and comparing the value of the first device until the value of the first signal substantially matches a predetermined value (Col. 5, lines 31-39; Col. 1, lines 26-55).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Jordan and Gonsalves to include the substep of modifying and comparing the value of the first device until the value of the first signal substantially matches a predetermined value as suggested by Davis. Davis cites Horowitz (US005254883A) as prior art (Col. 1, lines 26-29), and Horowitz describes that this method is advantageous because it makes sure that the current is always the same regardless of load and operating conditions (Col. 1, lines 58-60), and it minimizes current variations when there are variations in supply voltage, temperature, and processing (Col. 2, lines 40-43). Current variations lead to voltage level variations, and voltage variations can in turn lead to erroneous reading, which can result in the loss of data and other errors (Col. 2, lines 13-20), so this method is advantageous in that it avoids current variations.

29. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Normile (US005461679A) in view of Taylor (US006118461A).

Normile describes a video driver system comprising a first graphics device (401, Figure 4, *video processing module*, Col. 9, lines 11-15) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (412) to provide a first video output component signal (*modules 401-404 are coupled to a computer system bus 425 via control bus 412...coupled to system bus 425 is display controller 426...information is placed onto bus 425 by modules 401-404 and read in by display controller*

426, Col. 9, lines 15-24); a second graphics device (402, *video processing module*, Col. 9, lines 11-15) having an input from host (410, *first bus couples the compute modules and a host processor*, Col. 7, lines 48-49) and a first video component output (412) to provide a first video output component signal; a first video output port (425) coupled to the first video component output of the first graphics device and the first video component output of the second graphics device (*modules 401-404 are coupled to a computer system bus 425 via control bus 412...coupled to system bus 425 is display controller 426...information is placed onto bus 425 by modules 401-404 and read in by display controller 426*, Col. 9, lines 15-24); and a second video output port (440) coupled to the first video component output of the second graphics device (Col. 10, lines 7-19).

However, Normile does not teach that the first graphics device renders a frame of video and provides the rendered frame to the first video output port, and that the second graphics device renders an adjacent frame of video and provides the adjacent frame to the first video output port. However, Taylor describes two display control units (103, Figure 1, Col. 4, lines 14-18), and each display control unit includes a display controller (104) and a frame buffer (105) (Col. 4, lines 19-21). A display controller is a VGA controller (Col. 4, line 49) and executes a limited number of graphics functions such as line draws, polygon fills, color space conversion, display data interpolation and zooming (Col. 4, lines 52-57). Taylor describes that the frame from the frame buffer of display control unit 103a (Col. 5, line 65-Col. 6, line 1) is output first to the display (110) (Col. 6, lines 50-61), then the frame from the frame buffer of display control unit 103b (Col. 5, line 65-Col. 6, line 1) is output next to the display (Col. 7, lines 11-30). Therefore, Taylor describes that the first graphics device renders a frame of video and provides

the rendered frame to the first video output port, and that the second graphics device renders an adjacent frame of video and provides the adjacent frame to the first video output port.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Normile so that the first graphics device renders a frame of video and provides the rendered frame to the first video output port, and that the second graphics device renders an adjacent frame of video and provides the adjacent frame to the first video output port as suggested by Taylor because Taylor suggests that this increases the speed of the display system and is advantageous in the design and implementation of high speed/high resolution display systems (*multiple display controllers and/or frame buffers are used to independently drive corresponding regions on a display screen. Such application may be particularly advantageous in the design and implementation of high speed/high resolution display systems*, Col. 3, lines 34-39).

30. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US006118461A) in view of Wunner (US005095280A).

Taylor describes at least one digital to analog converter (109, Figure 1) operatively coupled to output video (*digital to analog converter 109...outputs the analog data to drive display 110*, Col. 5, lines 1-3).

However, Taylor does not teach having voltage adjusted in order to correlate video out voltages being provided by at least one of the graphics devices. However, Wunner describes a first graphics device (100, Figure 1), a second graphics device (102), and a common port (110), operatively coupled to receive the video from either of the first and second graphics devices.

Wunner describes having voltage adjusted in order to correlate video out voltages being provided by at least one of the graphics devices (*the VCO to adjust up or down to the new selected frequency*, Col. 8, lines 1-14).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Taylor so that the voltage is adjusted in order to correlate video out voltages being provided by at least one of the graphics devices as suggested by Wunner. This is well-known in the art and can be found in many applications, such as Deering, which will be described in the rejection for Claim 33. Deering suggests that a system utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in the viewed images because the computers do not operate from a single timing reference (Col. 3, lines 12-18). Wunner describes that adjusting the frequency means adjusting the voltage (*the VCO to adjust up or down to the new selected frequency*, Col. 8, lines 1-14). Therefore, it would be advantageous for the voltage to be adjusted in order to correlate video out voltages being provided by at least one of the graphics devices to avoid exhibiting aberrations in the viewed images.

31. Claims 33, 34, 36, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US006118461A) in view of Deering (US005963200A).

32. With regard to Claim 33, Taylor is relied upon for the teachings as discussed above relative to Claim 30.

However, Taylor does not teach a circuitry operative to provide digital to analog conversion voltage equalization associated with the first and second graphics devices. However, Deering describes an apparatus for providing video signals comprising a first graphics device (14, Figure 2) operative to render a first frame of video and a second graphics device (14) operative to render a second frame of video. Deering describes a circuitry operative to provide digital to analog conversion frequency equalization (*synchronizes events produced in the video timing generator circuits of the three RAMDACs*, Col. 5, lines 12-16). The frequencies produced by the RAMDACs will vary within a range of values which depends on voltage (Col. 4, lines 57-63). Wunner describes that adjusting the frequency means adjusting the voltage (*the VCO to adjust up or down to the new selected frequency*, Col. 8, lines 1-14). Therefore, Deering describes a circuitry operative to provide digital to analog conversion voltage equalization.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Taylor to include a circuitry operative to provide digital to analog conversion voltage equalization associated with the first and second graphics devices as suggested by Deering because Deering suggests that a system utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in the viewed images because the computers do not operate from a single timing reference (Col. 3, lines 12-18). Therefore, it is advantageous to include a circuitry operative to provide digital to analog conversion frequency or voltage equalization because it avoids exhibiting aberrations in the viewed images.

33. With regard to Claim 34, Taylor describes selecting video from the second graphics device (103b, Figure 1) to be output to the common port (*display driver 109 receives digital data from controller 104, Col. 5, lines 1-3, MAP OUT port of display unit 103b is then set active*, Col. 7, lines 25-30).

However, Taylor does not teach that the first graphics device includes a controller operative to select video from the second graphics device to be output. However, Deering describes a master graphics device and a slave graphics device (Col. 5, lines 22-25). The master graphics device emits the FIELD signal and the slave graphics device receives it (Col. 5, lines 25-27). The slave graphics device responds to the received FIELD signal by resetting the counters which produce the video timing signals (Col. 5, lines 30-33). Therefore, Deering describes that the first graphics device includes a controller operative to select video from the second graphics device to be output.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Taylor so that as suggested by Deering because Deering suggests that this is how a master-slave system works (Col. 5, lines 22-33). Deering suggests that a master-slave system is advantageous because the master provides a single timing reference (Col. 5, lines 22-45). A system utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in the viewed images because the computers do not operate from a single timing reference (Col. 3, lines 12-18). Therefore, because the master provides a single timing reference, this method avoids exhibiting aberrations in the viewed images.

34. With regard to Claim 36, Taylor does not teach that the first graphics devices acts as a master to the second graphics device and provides synchronization control for the second graphics device. However, Deering describes that the first graphics device (14, Figure 2) acts as a master to the second graphics device (14) and provides synchronization control for the second graphics device (Col. 5, lines 22-45).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Taylor so that the first graphics devices acts as a master to the second graphics device and provides synchronization control for the second graphics device as suggested by Deering because Deering suggests the advantage that the master provides a single timing reference (Col. 5, lines 22-45). A system utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in the viewed images because the computers do not operate from a single timing reference (Col. 3, lines 12-18). Therefore, because the master provides a single timing reference, this method avoids exhibiting aberrations in the viewed images.

35. With regard to Claim 37, Taylor does not teach that the first graphics device includes a reference signal generator for the second graphics controller. However, Deering describes that the first graphics devices includes a reference signal generator for the second graphics controller (*system 1 becomes the source of the vertical interval timing reference*, Col. 5, lines 22-45), as discussed in the rejection for Claim 36.

36. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US006118461A) in view of Eichenberger (see Prior Art of Record below).

Taylor is relied upon for the teachings as discussed above relative to Claim 30.

However, Taylor does not teach a load operatively couplable to either one of first and second graphics devices when at least one of the first and second graphics devices is not driving the common port. However, Eichenberger describes the use of a dummy switch with a load coupled to it for charge cancellation of the active switch (pp. 257, 260). In other words, the switch that is not active or is not driving the common port acts as the dummy switch and has a load coupled to it.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Taylor to include a load operatively couplable to either one of first and second graphics devices when at least one of the first and second graphics devices is not driving the common port as suggested by Eichenberger because Eichenberger suggests the advantage of reducing charge injection by charge cancellation (page 257). The advantages of using dummy switches is well-known in the art and can be found in many publications.

Allowable Subject Matter

37. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

38. The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken singly or in combination do not teach or suggest a method comprising the step of removing the first signal from the first node prior to the step or providing the second signal as recited in Claim 20. This claim is similar to Claim 19 of U.S. patent 6,424,320, to which this application is a continuation of.

Prior Art of Record

C. Eichenberger, W. Guggenbuhl, "On Charge Injection in Analog MOS Switches and Dummy Switch Compensation Techniques," *IEEE Transactions on Circuits and Systems*, vol. 37, pp. 256-264, 1990.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kehlet (US005956046A) describes a video system comprising a first frame buffer (202A, Figure 3) having an input (Col. 5, lines 49-51) and a first video component output (222A) to provide a first video output component signal (Col. 5, lines 51-53); a second frame buffer (202B) having an input (Col. 5, lines 49-51) and a first video component output (222B) to provide a first video output component signal (Col. 5, lines 51-53); a first video output port (220) coupled to the first video component output of the first frame buffer and to the first video component output of the second frame buffer (Col. 5, lines 51-53); wherein the first frame buffer has a rendered frame of video and provides the rendered frame to the first video output port, and wherein the second frame buffer has a rendered adjacent frame of video and provides the adjacent frame to the first video output port (Col. 6, lines 13-22).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Kee M. Tung
Primary Examiner